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14. ABSTRACT
The goal of this work has been to develop nanoscale VCSELs for integration into various optical systems, including for mounting on silicon. The nanoscale VCSELs can achieve small optical modes and present a compact laser diode that is also robust. In this work we have used a lithographic design and fabrication to realize a new type of VCSEL that is oxide free. Lithographic VCSELs as small as 1 μm diameter have been developed that deliver high power and low threshold. Slightly larger VCSELs of 2 μm size produce high efficiency, reaching 50 % power conversion efficiency. Stress testing has shown that the new VCSEL can produce reliability that exceeds commercial oxide

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Report Title

Final Report: WDM Nanoscale Laser Diodes for Si Photonic Interconnects

ABSTRACT

The goal of this work has been to develop nanoscale VCSELs for integration into various optical systems, including for mounting on silicon. The nanoscale VCSELs can achieve small optical modes and present a compact laser diode that is also robust. In this work we have used a lithographic design and fabrication to realize a new type of VCSEL that is oxide free. Lithographic VCSELs as small as 1 μm diameter have been developed that deliver high power and low threshold. Slightly larger VCSELs of 2 μm size produce high efficiency, reaching 50 % power conversion efficiency. Stress testing has shown that the new VCSEL can produce reliability that exceeds commercial oxide VCSELs.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received		Paper
08/31/2013	4.00	Y. Zhang, D. G. Deppe, K. Konthasinghe, A. Muller, G. Zhao. Buried heterostructure vertical-cavity surface-emitting laser with semiconductor mirrors, Applied Physics Letters, (09 2012): 0. doi: 10.1063/1.4750062
08/31/2015	11.00	Ming Xin Li, Xu Yang, Dennis G. Deppe, Guowei Zhao, Sabine Freisem. Small oxide-free vertical-cavity surface-emitting lasers with high efficiency and high power, Electronics Letters, (11 2014): 0. doi: 10.1049/el.2014.3352
08/31/2015	10.00	D.G. Deppe, M. Li, S. Freisem, X. Yang, Y. Zhang, G. Zhao. Oxide-free vertical-cavity surface-emitting lasers with low junction temperature and high drive level, Electronics Letters, (09 2014): 0. doi: 10.1049/el.2014.2626
TOTAL:		**3**

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received		Paper
09/08/2014	9.00	J.M. Dallesasse, D.G. Deppe. III-V Oxidation: Discoveries and Applications in Vertical-Cavity Surface-Emitting Lasers, Proceedings of the IEEE, (12 2012): 0. doi:
TOTAL:		**1**

Number of Papers published in non peer-reviewed journals:

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received		Paper
07/22/2016	1.00	D.G. Deppe, M. Li, X. Yang. Metal Cavities as the Efficiencyy Killer in Nanolaser and Spontaneous Light Sources, Conference on Lasers and Electro-Optics. 11-JUN-13, San Jose, CA. : ,
07/22/2016	2.00	G. Zhao, X. Yang, Y. Zhang, M. Li, D.G. Deppe, C. Cao, J. Thorp, P. Thiagarajan, M. McElinney. Record Low Thermal Resistance of Mode-Confined VCSELs using AlAs/AlGaAs DBRs, Conference on Lasers and Electro-Optics. 11-JUN-13, San Jose, CA. : ,
07/22/2016	3.00	Y. Zhang, M. Li, D. Deppe, G. Zhao, X. Yang. Nanoscale VCSELs: Thermal Properties and Current Drive Levels and Their Contrast to Other Nanoscale Diode Laser Approaches, GOMACTech. 11-MAR-13, Las Vegas, NV. : ,
07/22/2016	7.00	D.G. Deppe, Y. Zhang, G. Zhao, X. Yang, X. Liu, M. Li. Letting the heat out: Integration of VCSELs with Si, IEEE OPTICAL INTERCONNECTS CONFERENCE 2014. 06-MAY-14, Coronado, CA. : ,
07/22/2016	6.00	G. Zhou, D.G. Deppe, X. Yang, Y. Zhang, X. Liu, M. Li. Scaling VCSEL Arrays to High Power and High Speed: Importance of the Buried Heterostructure, 2014 GOMACTech. 18-MAR-14, Charleston, SC. : ,
07/22/2016	14.00	Dennis Deppe, Mingxin Li, Guowei Zhao, Xu Yang. Impact of VCSEL Scaling on Speed and BIt Energy for High Speed Interconnects, IEEE Summer Topicals 2015. 13-JUL-15, Nassau. : ,
TOTAL:	**6**	

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received		Paper
07/22/2016	8.00	X. Yang, G. Zhao, M. Li, X. Liu, Y. Zhang, D.Deppe. 50% Power Conversion Efficiency in Non-Oxide VCSELs, 2014 Conference on Lasers and Electro Optics. 13-JUN-14, San Jose, CA. : ,
07/22/2016	12.00	Dennis Deppe, Xu Yang, Yu Zhang, Guowei Zhao, Mingxin Li. Universal Reliability Model for VCSELs and Other Laser Diodes, SPIE Photonics West. 07-FEB-15, San Jose, CA. : ,
07/22/2016	13.00	Dennis Deppe, Guowei Zhao, Xu Yang, Yu Zhang, Xiahong Liu, Mingxin Li. Small Sized VCSELs, SPIE Photonics West. 07-FEB-15, San Jose, CA. : ,
TOTAL:		**3**

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received		Paper
07/22/2016	5.00	X. Yang, M. Li, G. Zhao, Y. Zhang, S. Freisem, D.G. Deppe. Oxide-free vertical-cavity surface-emitting lasers with low junction temperature and high drive level, Electronics Letters (06 2014)
TOTAL:		**1**

Number of Manuscripts:

Books

Received	Book
TOTAL:	

Received	Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

Four invited talks were presented on the results for this project.

Graduate Students

NAME	PERCENT_SUPPORTED	Discipline
G. Zhao	0.50	
Y. Zhang	0.50	
X. Liu	0.50	
X. Yang	0.50	
M. Li	0.50	
FTE Equivalent:	**2.50**	
Total Number:	**5**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Dennis Deppe	0.08	
FTE Equivalent:	**0.08**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):.....	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Total Number:

Names of personnel receiving PHDs

NAME	
G. Zhao	
Y. Zhang	
X. Liu	
Total Number:	**3**

Names of other research staff

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

Technology Transfer

There have been strong interactions with industry for the VCSEL technology of this project. Related to the project was work with Lasertel, Inc. which also supported research into the technology for high power arrays. Interactions with Boeing has led to additional support through AFRL for the high reliability aspect of the VCSELs. This interaction continues for high speed interconnects with new proposals being planned to incorporate the VCSELs into their systems. Finisar has performed fabrication of 3" VCSEL wafers based on the technology. sdPhotonics is a UCF spin-off based on the VCSELs that has gained further support from ARL through SBIRs. The development of the technology has continued through an additional project with the ARO to develop very high speed. This project is underway and progressing with a great deal of interest in 50 Gbps data links for data centers and high performance computers.

Final Report:

WDM Nanoscale Laser Diode for Si Photonic Interconnects

P.I.: Dennis G. Deppe, Professor, UCF

Statement of the problem studied:

This project has been to develop a new type of laser that is a vertical-cavity surface-emitting laser (VCSEL) with semiconductor mirrors and an electronic and optical confinement scheme that enable scaling to small size. The new VCSEL defines the laser cavity and electrical injection lithographically in a self-aligned fashion, and has been shown to enable small and efficient lasers that are difficult to achieve by other means. The lateral confinement is much stronger than other known techniques for making VCSELs, and enables scaling to submicron dimensions.

The new VCSEL termed a lithographic VCSEL is particularly attractive for integration with silicon. The VCSEL size can be made sufficiently small to couple to waveguides formed on silicon platforms, such as SiN on SiO2, or other materials. The VCSEL also has key features needed for high speed, including low thermal resistance, high reliability enabling high drive level, and the potential for high speed.

Summary of the most important results:

Several breakthroughs were made on developing practical VCSELs that could reach nanoscale dimensions. The VCSEL size has been reduced to micron dimensions, nearly into the nanoscale regime. The project has resulted in a number of record results including record high power conversion efficiency, record low different resistance, record low thermal resistance, and record high power for the given laser volume. Many of these results are entertwined and result from the internal confinement mechanism.

Figure 1 shows the difference between the standard oxide-confined VCSEL and the new laser technology based on internal epitaxial confinement. The new laser uses a lithographically defined conducting channel into the laser active region. The new VCSELs have been scaled to diameters of 1 μm, while retaining high efficiency and high reliability.[1] It uses an internal conducting channel to the active region to lower electrical resistance. Modeling shows that advantages in internal heat flow and electrical parasitics are enabling for single channel speed in excess of 100 Gbps in arrays with laser spacing as small as 50 μm.

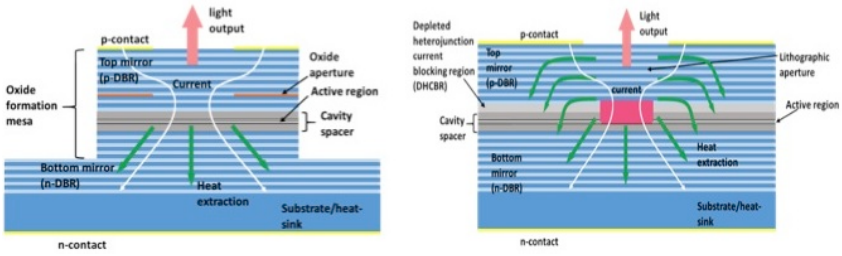

Fig. 1 (a) and (b) contrast the oxide VCSEL now used as the short reach (SR) interconnects with the lithographic VCSEL of this project.

Because the new VCSEL eliminates the oxide aperture and enables the upper mirror to use AlAs low index layers it can achieve very low thermal resistance. Moreover our intention is in developing a technology for commercial impact in the near term, as well as a technology base to produce nanolasers that can lead to new applications based on future developments. High speed and silicon integration are two of these. The new VCSEL technology exceeds oxide VCSEL performance for next generation technologies that need laser sizes ranging from 6 µm to 2 µm, can be used in densely integrated arrays, and for applications in pumping, free space interconnects, and sensors.

We know that laser speed and bit energy track the laser size. VCSELs are now the fastest lasers demonstrated, and both intrinsic response and electrical parastics contribute almost equally to the response. Figure 3 shows the electrical parasitics of the new VCSEL technology. Minimizing contacting and aperture dimensions due to the nearly planar processing while retaining low differential resistance will produce the highest electrical bandwidth yet for a laser. Electrical bandwidth is estimated at over 80 GHz for the 2.5 µm aperture. Analysis of the intrinsic speed based on heat flow and drive level presented in Fig. 4 indicates that intrinsic laser response can reach 100 GHz because of reduced heating. Direct modulation data rate can be greater than 100 Gbps. The oxide VCSEL shown in Fig. 2 is limited electrically by the deep mesa size needed to form the oxide aperture that sets capacitance, and the electrical resistance of the oxide aperture.

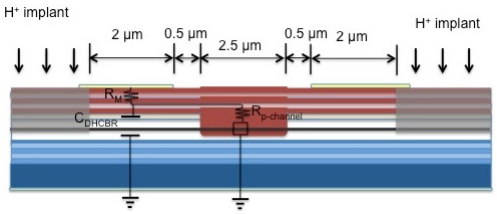

Fig. 3 Schematic showing electrical parasitics for a 2.5 µm diameter lithographic VCSEL.

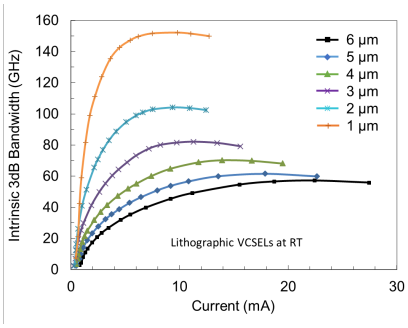

Fig. 4 Extracted intrinsic bandwidth from CW VCSEL measurements.

The electrical resistance is reduced due to the electrically conducting channel created in the cavity spacer, and parasitic capacitance is reduced due to the small VCSEL size and contact area. Standard proton implant will be used minimize capacitance outside the metal contacting region. The effective capacitance region shown in Fig. 3 is reduced to $4x10^{-7}$ cm^2 and can produce capacitance < 15 fF. Simulation indicates that combined electrical and intrinsic bandwidth will be increased to more than 100 Gbps using standard processing and stepper alignment for a bias current of only 2 mA. The small VCSEL can be coupled to multimode or single mode waveguides, and be inserted directly into existing transceiver packages.

Figure 5 shows a light vs. current curve (left) and voltage vs. current (right) curves for a 6 µm diameter VCSEL showing threshold, output power, and differential resistance for the new VCSEL technology relative to the best results for oxide VCSELs. The differential resistance is only 43 ohms. The maximum power is over 17 mW due to the low thermal resistance. These parameters measured on the project are among the best if not the best that have been achieved for lasers of this size.

	Ith (mA)	P_max(mW)	slope eff.	wall-plug eff.	Volt at 10kA/cm2
6μm	0.89	17.18	61.4%	38.9%	1.458

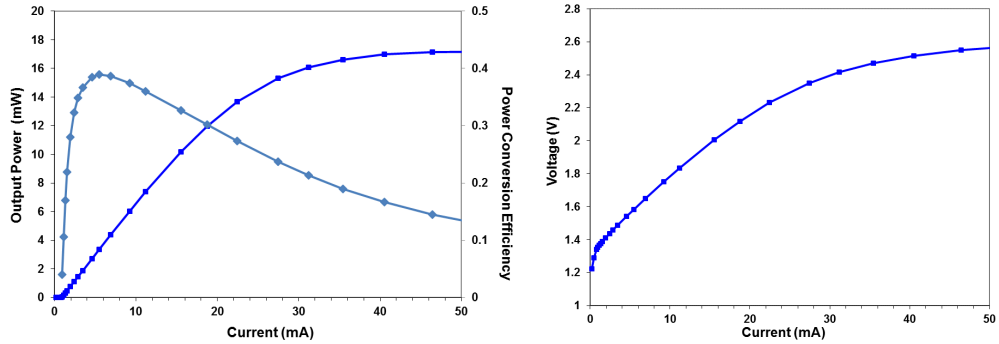

Fig. 5 On the left is shown the light vs. current curve for a 6 μm lithographic VCSEL and on the right is shown the voltage vs. current curve. The maximum output power is 17 mW and the differential resistance is only 43 ohms.

Figure 6 shows the light vs. current curves for smaller VCSELs. These powers for the VCSEL sizes are record high, and power conversion efficiencies are close to 50%. Notably the 1 μm diameter VCSEL delivers approximately 5 mW of maximum power. While the powers decrease as the VCSELs gets smaller, as expected, the power density goes up. This increasing power density with reducing size is due to less total power dissipated, and less heating for a given power density. Also notable is that the slope efficiency remains nearly constant with size even down to the 1 μm diameter size. This indicates that smaller VCSELs fabricated for example using finer lithography are indeed possible with this technology and can produce high quality lasers.

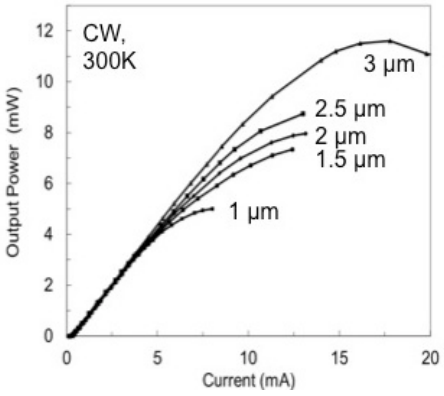

Fig. 6 Light vs. current curves measured CW at room temperature for lithographic VCSEL sizes ranging from 3 μm to 1 μm diameter. The slope efficiency remains nearly constant for the different laser sizes. The power from each size represent to our knowledge record values.

Reliability for 3 μm diameter VCSELs has also been tested under this project and compared with oxide VCSELs of the same size.[2] The results are shown in Fig. 7. The test conditions correspond to 150 kA/cm^2 and 150 C stage temperature. The results for three lithographic VCSELs are shown in solid curves and the results for two commercial oxide VCSELs are shown in dashed curves. The lower junction temperatures for the lithographic VCSELs make the lithographic VCSELs more reliable. Therefore these VCSELs can be driven to very high level reliably, needed for high speed operation.

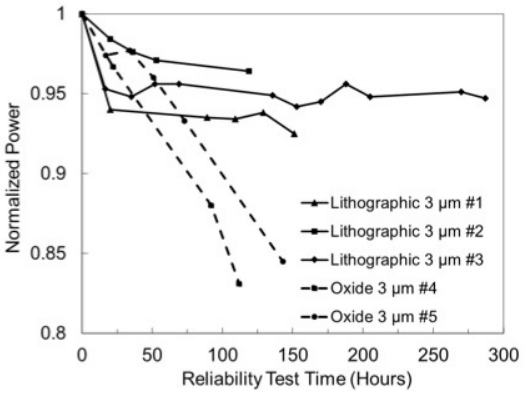

Fig. 7 Normalized power vs. time for 3 µm diameter lithographic VCSELs (solid curves) and 3 µm diameter commercial oxide VCSELs (dashed curves). The stress testing is done at 150 C and 150 kA/cm2 current density (10 mA bias). The lithographic VCSELs are more reliable under the stress conditions than oxide VCSELs.

Finally in this report we show results in Fig. 8 from simulations of intrinsic laser speed based on measured continuous-wave light vs. current curves that account for internal heating. This internal heating ultimately limits the bandwidth of oxide VCSELs for high temperature operation, due to thermal rollover. Also shown is the footprint that can be achieved with this laser technology due to its planar surface.

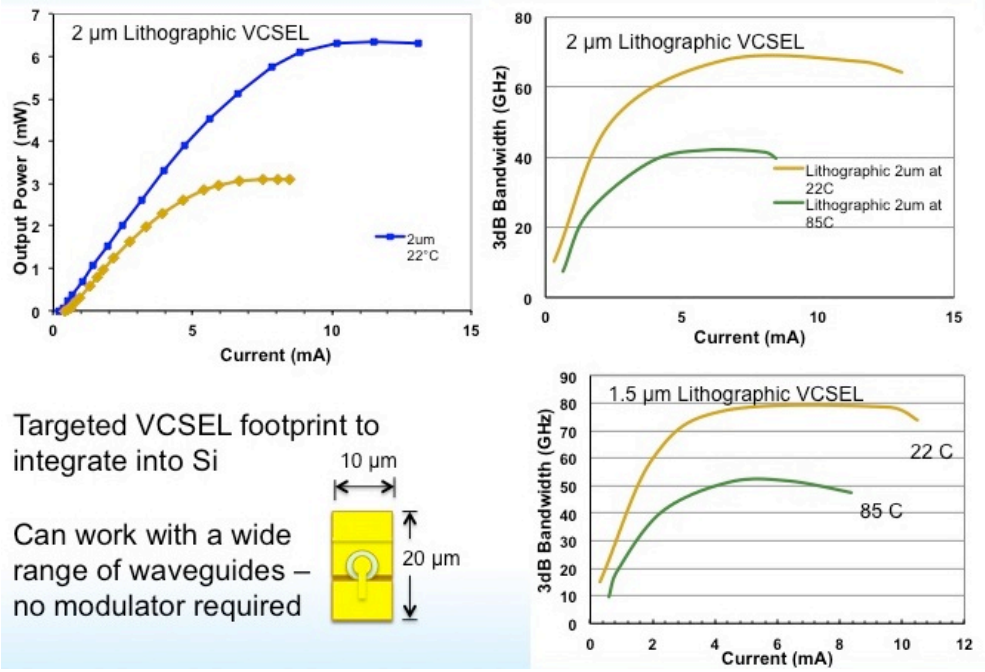

Fig. 8 Upper left shows the light vs. current curve at 22 C and 85 C for a 2 µm VCSEL. The upper right shows simulated intrinsic speed based on the CW L-I's measured for the 2 µm. The lower right shows the simulated intrinsic speed based on CW L-I's measured for a 1. 5 µm VCSEL. The lower left shows an image of a VCSEL chip with electrical contacting designed for flip-chip mounting onto a platform such as silicon.

In the upper left plot are shown the measured L-I's for a 2 µm VCSEL for measurements at either 22 C (blue curve) or 85 C (yellow curve). Internal temperatures vs. current are extracted for both 22 C and 85 C and used to determine the intrinsic modulation speed from simulation. The results in the upper right show the modeled

modulation speed for the 2 μm VCSEL. The 85 C small signal response is modeled to reach its maximum at about 5 mA and estimated at just over 40 GHz. Room temperature small signal response is estimated at approximately 70 GHz at 8 mA. The modeling show that stimulated emission rate, or photon density in the cavity, is the limiting mechanism for intrinsic speed, as opposed to differential gain that may reduce due to heating.

Modeled results for a smaller VCSEL are shown on the lower right. The VCSEL in this case has 1.5 μm diameter, and the small signal model is again extracted from the measured CW L-I's. Because of reduced heating, the smaller VCSEL shows an intrinsic speed of over 50 GHz (from modeling) at 85 C. Again the maximum intrinsic speed is predicted to be limited by the maximum photon density as opposed to differential gain.

In the lower left is shown the footprint that is estimated to be possible with the new technology. It is believed that the VCSEL could be as small as 10 μm x 20 μm for integration into various platforms such as silicon. This can allow close coupling with silicon electronic drive and control circuitry for a range of applications.

The project has gained the interest of additional agencies and industrial collaborators. A strong interest is in the high speed potential for small VCSELs that can reduce the bit energy and be used for dense integration. Work continues in developing the high-speed fabrication process for the new VCSEL technology. Further work has also been performed in reliability. Working in collaboration, Finisar has now demonstrated high reliability in 5 μm diameter VCSELs.

References:

[1] X. Yang, M. Li, G. Zhao, S. Freisem, and D. Deppe, "Small oxide-free vertical-cavity surface-emitting lasers with high efficiency and high power," Electron. Lett. 50, 1864 (2014).

[2]X. Yang, G. Zhao, M. Li, and D. Deppe, "Stress test of lithographic vertical-cavity surface-emitting lasers under extreme operating conditions," Electron. Lett. 51, 1279 (2015).